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Equivalent of Form PTO/SB/08b (08-08)

Substitute for 1449/PTO		Complete if Known			
FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	09/788,670		
		Filing Date	February 21, 2001		
		First Named Inventor	Hartvig W.J. EKNER		
		Art Unit	2193		
		Examiner Name	Do, Chat C.		
Sheet	1	of	9	Attorney Docket Number	1778.2110000

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	NPL1	KUTLER, JEFFREY, <i>Smart Cards: Even Abundant Security Features Don't Spur Smart Card Buy-Ins</i> , AMERICAN BANKER, Vol. 163, No. 221, November 18, 1998, available in Am. Banker 11998 WL 13326041 (3 pages).	
	NPL2	STMicroelectronics And Gemplus Announce Smart Card Security Certification Including Hardware And Software, EDP WEEKLY'S IT MONITOR, Vol. 42, Issue 13, April 2, 2001, available in EDP Wkly. 42001 WL 14018034 (3 pages).	
	NPL3	Can Silicon Stop the Smartcard Hackers? ELECTRONIC TIMES, February 15, 1999, available in Electronics Times 321999 WL 9348105 (2 pages).	
	NPL4	STMicroelectronics And Gemplus Announce Smart Card Security Certification Including Hardware and Software, BUSINESS WIRE, March 29, 2001, available in WESTLAW, 3/29/01 Bus. Wire 02.05.00 (3 pages).	
	NPL5	VOLLMER, A., <i>Security ICs Are Targeting Consumer Applications</i> , ELECTRONIC DESIGN, Vol. 48, Issue 23, November 6, 2000, available in Electronic Design 1052000 WL 14003957 (13 pages).	
	NPL6	CORON, J.-S. and GOUBIN, L., "On Boolean and Arithmetic Masking Against Differential Power Analysis," in <i>Proceedings of Second International Workshop on Cryptographic Hardware and Embedded Systems, CHES 2000</i> (Eds., C.K. Koc and C. Paar), Worcester, Massachusetts, USA, August 17-18, 2000, pp. 231-237, Springer-Verlag, Berlin/Heidelberg, Germany (2000).	
	NPL7	HASAN, M. ANWAR, "Power Analysis Attacks and Algorithmic Approaches to their Countermeasures for Koblitz Curve Cryptosystems," in <i>Proceedings of Second International Workshop on Cryptographic Hardware and Embedded Systems, CHES 2000</i> (Eds., C.K. Koc and C. Paar), Worcester, Massachusetts, USA, August 17-18, 2000, pp. 93-108, Springer-Verlag, Berlin/Heidelberg, Germany (2000).	
	NPL8	KATO, T. et al., "A Design for Modular Exponentiation Coprocessor in Mobile Telecommunication Terminals," in <i>Proceedings of Second International Workshop on Cryptographic Hardware and Embedded Systems, CHES 2000</i> (Eds., C.K. Koc and C. Paar), Worcester, Massachusetts, USA, August 17-18, 2000, pp. 216-228, Springer-Verlag, Berlin/Heidelberg, Germany (2000).	
	NPL9	MAYER-SOMMER, R., "Smartly Analyzing the Simplicity and the Power of Simple Power Analysis on Smartcards," in <i>Proceedings of Second International Workshop on Cryptographic Hardware and Embedded Systems, CHES 2000</i> (Eds., C.K. Koc and C. Paar), Worcester, Massachusetts, USA, August 17-18, 2000, pp. 78-92, Springer-Verlag, Berlin/Heidelberg, Germany (2000).	
	NPL10	NACCACHE, D. and TUNSTALL, M. "How to Explain Side-Channel Leakage to Your Kids," in <i>Proceedings of Second International Workshop on Cryptographic Hardware and Embedded Systems, CHES 2000</i> (Eds., C.K. Koc and C. Paar), Worcester, Massachusetts, USA, August 17-18, 2000, pp. 229-230 Springer-Verlag, Berlin/Heidelberg, Germany (2000).	
Examiner Signature	/Chat Do/	Date Considered	05/26/2009

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Substitute for form 1449/PTO

Complete if Known**FOURTH SUPPLEMENTAL
INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet	2	of	9	Application Number	09/788,670
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Filing Date	February 21, 2001
First Named Inventor	Hartwig W.J. EKNER
Art Unit	2193
Examiner Name	Do, Chat C.
Attorney Docket Number	1778.2110000

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T ²
	NPL11	SHAMIR, A., "Protecting Smart Cards from Passive Power Analysis with Detached Power Supplies," in <i>Proceedings of Second International Workshop on Cryptographic Hardware and Embedded Systems, CHES 2000</i> (Eds., C.K. Koc and C. Paar), Worcester, Massachusetts, USA, August 17-18, 2000, pp. 71-77 Springer-Verlag, Berlin/Heidelberg, Germany (2000).	
	NPL12	WEINGART, S.H., "Physical Security Devices for Computer Subsystems: A Survey of Attacks and Defenses," in <i>Proceedings of Second International Workshop on Cryptographic Hardware and Embedded Systems, CHES 2000</i> (Eds., C.K. Koc and C. Paar), Worcester, Massachusetts, USA, August 17-18, 2000, pp. 302-317, Springer-Verlag, Berlin/Heidelberg, Germany (2000).	
	NPL13	KOCHER, P. et al., "Differential Power Analysis," in <i>Advances in Cryptology - Proceedings of 19th Annual International Cryptology Conference, CRYPTO '99</i> (Ed. Michael I. Wiener), Santa Barbara, California, USA, August 15-19, 1999, Springer-Verlag, Berlin/Heidelberg, Germany (1999) Pages 388-397.	
	NPL14	DAEMEN, J. et al., "Bitslice Ciphers and Power Analysis Attacks," presented at <i>Fast Software Encryption Workshop 2000</i> , New York, New York, USA, April 10-12, 2000 (16 pages).	
	NPL15	CLAVIER, C. et al., "Differential Power Analysis in the Presence of Hardware Countermeasures," in <i>Proceedings of Second International Workshop on Cryptographic Hardware and Embedded Systems, CHES2000</i> (Eds., C.K. Koc and C. Paar), Worcester, Massachusetts, USA, August 17-18, 2000, pp. 252-263 Springer-Verlag, Berlin/Heidelberg, Germany (2000).	
	NPL16	SHI, Z., et al., "Bit Permutation Instructions for Accelerating Software Cryptography," <i>Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors</i> , pp.138-148, Boston, MA (July 10-12, 2000).	
	NPL17	Marketing literature from Philips Semiconductors, "On the Move - Philips Semiconductors and IBM Research to Co-develop Secure Smart Cards" [online]. February 1999, Document order number 9397.750.05157, [Retrieved on 2006-02-01]. Retrieved from the Internet: <URL: http://www.semiconductors.philips.com/acrobat/download/literature/9397/75005157.pdf >	
	NPL18	Philips Semiconductors Short Form Specification, "P16WX064 SmartXA-Family, Secure 16-bit Smart Card Controller," Revision 1.1 [online], February 2001, pp. 1-11 [Retrieved on 2006-02-01]. Retrieved from the Internet: <URL: http://www.semiconductors.philips.com/acrobat/download/other/identification/sfs052411.pdf >	
	NPL19	Certification Report BSI-DSZ-CC-0203-2003 for Philips Smart Card Controller P16WX064VOC [online]. Philips Semiconductors GmbH [Retrieved on 2006-02-01]. Retrieved from the Internet: <URL: http://www.bsi.bund.de/zertifiz/zert/report/0203a.pdf >	
	NPL20	"Security Target BSI-DSZ-CC-0203, Version 1.1, January 24th, 2003, Evaluation of the Philips P16WX064VOC Secure 16-bit Smart Card Controller" [online]. Philips Semiconductors GmbH, pp. 1-74 [Retrieved on 2006-02-01]. Retrieved from the Internet: <URL: http://www.commoncriteriportal.org/public/files/cpfiles/0203b.pdf >	

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				<i>First Named Inventor</i>	Hartvig W.J. EKNER
				<i>Art Unit</i>	2193
				<i>Examiner Name</i>	Do, Chat C.
Sheet	3	of	9	<i>Attorney Docket Number</i>	1778.2110000

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T ²
	NPL21	CASE, B., "Superscalar Techniques: SuperSPARC vs. 88110," <i>Microprocessor Report</i> , Vol. 5, No. 22, December 4, 1991, pages 1 and 6-11.	
	NPL22	DIEFENDORFF, K., "The 88110: A Superscalar Microprocessor with Graphics Support" (Motorola), <i>Microprocessor Forum</i> , November 1991, 20 pages (Bates Numbers L00622-00641).	
	NPL23	EYRE, J., et al., "Infineon's TriCore Tackles DSP," <i>Microprocessor Report</i> , April 19, 1999, pp. 12-14.	
	NPL24	FEIGEL, C.P., "TI Introduces Four-Processor DSP Chip," <i>Microprocessor Report</i> , March 28, 1994, pages 22-25.	
	NPL25	GWENNAP, L., "Intel's MMX Speeds Multimedia," <i>Microprocessor Report</i> , MicroDesign Resources, Vol. 10, No.3, March 5, 1996, 6 Pages.	
	NPL26	GWENNAP, L., "New Multimedia Chips to Enter the Fray," <i>Microprocessor Report</i> , MicroDesign Resources, Vol. 10, No. 13, October 1996, Page 9.	
	NPL27	HALFHILL, T.R. and BELGARD, R., "Mips vs. Lexra: Definitely Not Aligned," <i>Microprocessor Report</i> , Vol. 13, No. 16, December 6, 1999, pages 1-5.	
	NPL28	HEINRICH, J., <i>MIPS R4000 Microprocessor User's Manual</i> , Second Edition, MIPS Technologies, Inc., 1994, pages 154-155, 157, 159, 161, 168, 170-171, B-9, B-10, B-13, B-17, B-19, B-21, B-23, B-27, B-38, B-40, and B-62.	
	NPL29	KILLIAN, E., "MIPS Extensions for Digital Media," <i>Microprocessor Forum</i> , October 22-23, 1996, pages 1-5.	
	NPL30	TURLEY, J., "Siemens TriCore Revives CISC Techniques," <i>Microprocessor Report</i> , MicroDesign Resources, November 17, 1997, pages 13- 16.	

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	NPL31	WEISS, R., <i>ARM Piccolo Mixes ARM RISC with DSP</i> , at http://www.estd.com/Editorial/1996/11/Briefs/arm.html , 1 page (November 1996).	
	NPL32	<i>601 First Silicon</i> , at http://www.mot.com/SPSPowerPC/library/press_releases/601_First_Silicon.html , 2 pages (October 1, 1992).	
	NPL33	<i>AN1214: MC88110 64-bit External Bus Interface to 16-bit EPROM</i> , at http://www.mot-sps.com/lit/html/anL214.html , 1 page (January 24, 1997).	
	NPL34	<i>DSP56002 24-Bit Digital Signal Processor User's Manual</i> , Motorola, Inc., 1995, 386 pages (Bates Numbers L07277-L07662).	
	NPL35	<i>DSP56002/DSP56L002 Motorola Semiconductor Product Information</i> , Motorola, Inc., 1994, 3 pages (Bates Numbers L07913-L07915).	
	NPL36	<i>DSP56002 Semiconductor Technical Data</i> , Motorola, Inc., 1996, 110 pages (Bates Numbers L07803-L07912).	
	NPL37	<i>EB162: Programming Tips (MC88110)</i> , at http://www.mot-sps.com/lit/html/eb162.html , 1 page (January 24, 1997).	
	NPL38	<i>Hardware Implications of xmem as a st followed by a ld, Motorola Semiconductor Engineering Bulletin</i> , Motorola, September 1992, 5 pages.	
	NPL39	<i>Interrupt Latency in the MC88110, Motorola Semiconductor Engineering Bulletin</i> , Motorola, 1992, pages 1, 2 and 4-9.	
	NPL40	<i>An Introduction to Thumb™</i> , Version 2.0, Advanced RISC Machines, March 1995, 29 pages.	

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	NPL41	Lexra Announces Industry's First RISC-DSP Core Based on MIPS® Instruction Set Architecture, at http://www.lexra.com/pr_990505.html , 3 pages (May 5, 1999).	
	NPL42	Lexra Announces the Fastest 32-BIT RISC Core to Execute MIPS® Instructions*, at http://www.lexra.com/pr_990719.html , 2 pages (July 19, 1999).	
	NPL43	Lexra Announces the First Mainstream 32-bit RISC Core In a Programmable Logic Device, at http://www.lexra.com/pr_981005.html , 3 pages (October 5, 1998).	
	NPL44	Lexra Announces its LX4080 Evaluation System is Proven and Available for Production, at http://www.lexra.com/pr_980720.html , 2 pages (July 20, 1998).	
	NPL45	Lexra Announces LX4080 Embedded RISC Processor Core, Delivering High Performance & executes MIPS-I instructions set*, at http://www.lexra.com/pr980112.html , 2 pages (January 12, 1998).	
	NPL46	Lexra Announces LX4080 SmoothCore™ Silicon Proven RISC Core, at http://www.lexra.com/pr_980323.html , 3 pages (March 23, 1998).	
	NPL47	Lexra Announces Next Generation Embedded RISC Core, at http://www.lexra.com/pr_990111.html , 3 pages, (January 11, 1999).	
	NPL48	Lexra ASYM-LX Instruction Set Simulator Product Brief, date unknown, 2 pages.	
	NPL49	Lexra ASYM-LX Simulator/FIR Filter Demo, date unknown, 5 pages.	
	NPL50	Lexra Command Line User Environment (CLUE) for ASYM-LX User's Guide, Revision 1.1, January 28, 2000, pages 1-32.	

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	NPL51	<i>Lexra [Products]</i> , at http://www.lexra.com/lx-products2.html , 2 pages (Copyright 1998-1999).	
	NPL52	<i>Lexra Rolls Out Second MIPS Core (Lexra LX4180) (Product Announcement)</i> , <i>Microprocessor Report</i> , January 28, 1999, 1 page (printed from West database).	
	NPL53	<i>LX4080</i> , at http://www.lexra.com/lx4080.html , 8 pages (Copyright 1998-1999).	
	NPL54	<i>LX4080P</i> , at http://www.lexra.com/lx4080p.html , 6 pages (Copyright 1998-1999).	
	NPL55	<i>LX4280</i> , at http://www.lexra.com/lx4280.html , 2 pages (Copyright 1998-1999).	
	NPL56	<i>LX4280 Fills Lexra's Midrange (MIPS-compatible embedded processor core) (Product Announcement)</i> , <i>Microprocessor Report</i> , August 2, 1999, 1 page (printed from West database).	
	NPL57	<i>LX5280</i> , at http://www.lexra.com/lx5280.html , 2 pages (Copyright 1998-1999).	
	NPL58	<i>MC88110/410DH/AD: MC88410/MC88410 Designer's Handbook</i> , at http://www.mot-sps.com/lit/html/mc88110410dhad.html , 1 page (January 24, 1997).	
	NPL59	<i>MC88110UM/AD: MC88110 Second Generation RISC Microprocessor User's Manual</i> , at http://www.mot-sps.com/lit/html/mc88110umad.html , 1 page (January 24, 1997).	
	NPL60	<i>MC88410UM/AD: MC88410 Secondary Cache Controller User's Manual</i> , at http://www.mot-sps.com/lit/html/mc88410umad.html , 1 page (January 24, 1997).	

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	NPL61	<i>Microprocessor Devices Reliability Monitor Report: Third Quarter 1997</i> , Motorola, 8 pages (1997).	
	NPL62	<i>Microprocessor Devices Reliability Monitor Report: Fourth Quarter 1997</i> , Motorola, 10 pages (1997).	
	NPL63	<i>MIPS Technologies, Inc. Files Lawsuit to Protect Intellectual Property Rights</i> , at http://www.mips.com/pressReleases/102899B.html , 2 pages (October 28, 1999).	
	NPL64	<i>MIPS Technologies, Inc. Litigation Overview and Q&A</i> , at http://www.mips.com/pressReleases/102899D.html , 3 pages (visited February 24, 2000).	
	NPL65	<i>MIPS: Open Letter from John Bourgoign, CEO, MIPS Technologies</i> , at http://www.mips.com/pressReleases/102899C.html , 2 pages (visited February 24, 2000).	
	NPL66	<i>QML-DSP/MCM and Die Courier</i> , at http://www.ti.com/sc/docs/military/liter/ecour/dsp.htm , 7 pages (January 1996).	
	NPL67	<i>Reliability Monitor Environmental Stress Data 3Q97</i> , Motorola, 1997, 4 pages.	
	NPL68	<i>Reliability and Quality Report 3Q97</i> , Motorola, 1997, 2 pages.	
	NPL69	<i>Reliability and Quality Report 4Q97</i> , Motorola, 1997, 2 pages.	
	NPL70	<i>Running the MC88110 in Lockstep, Motorola Semiconductor Engineering Bulletin</i> , Motorola, 1992, 2 pages.	

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Substitute for form 1449/PTO				Complete if Known	
FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Application Number	09/788,670
				Filing Date	February 21, 2001
				First Named Inventor	Hartvig W.J. EKNER
				Art Unit	2193
				Examiner Name	Do, Chat C.
Sheet	8	of	9	Attorney Docket Number	1778.2110000

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T ²
	NPL71	TMS320C80 Digital Signal Processor, Texas Instruments, July 1984, 5 Pages.	
	NPL72	Digital Equipment Corporation, VAX 11/780 Architecture Handbook, 1977. pp. 6-26, 6-27, 6-30, 6-31.	
	NPL73	TANENBAUM, A.S., Structured Computer Organization, Prentice-Hall, Inc. 1984, pp. 10-12	
	NPL74	Fairchild CLIPPER™ 32-Bit Microprocessor User's Manual, Prentice-Hall, Inc., Englewood Cliffs, New Jersey (1987).	
	NPL75	Wikipedia article, "Finite field arithmetic", www.wikipedia.com , author unknown, retrieved July 30, 2008, 4 Pages.	
	NPL76	Wikibooks article, "Data Coding Theory/Modulo-2 Arithmetic", author unknown, retrieved July 30, 2008, 2 Pages.	
	NPL77	Galois Filed Arithmetic Library, www.partow.net/projects/galois/ 2 January 2006, 4 Pages.	
	NPL78	Clipper architecture: Information from Answers.com at http://www.answers.com/topic/clipper-architecture , 4 pages (retrieved July 25, 2006).	
	NPL79	DHEM, J.F and FEYT, N., "Hardware and Software Symbiosis Helps Smart Card Evolution" [online]. IEEE Micro, November-December 2001, pp. 14-25 [Retrieved on 2006-02-01]. Retrieved from the Internet: <URL: http://www.it.itb.ac.in/~satish/Thesis%20Report%20New%201/2_Review%20of%20literature/2_29_Hardware%20and%20software%20symbiosis%20helps%20smart%20card%20evolution.pdf >	
	NPL80	DHEM, J.F and FEYT, N., "Present and Future Smart Cards" [online]. Gemplus - Card Security Group, pp. 1-9 [Retrieved on 2006-02-01]. Retrieved from the Internet: <URL: http://www.it-c.dk/courses/DSK/F2003/smart2.pdf >	

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FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Application Number	09/788,670
				Filing Date	February 21, 2001
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T ²
	NPL81	KOC, C.K. and ACAR, T., "Montgomery Multiplication in GF (2 ⁿ). " Proceedings of Third Annual Workshop on Selected Areas in Cryptography, pp. 95-106, Queens University, Kingston, Ontario, Canada, August 15-16, 1996 (13 pages).	
	NPL82		
	NPL83		
	NPL84		
	NPL85		
	NPL86		
	NPL87		
	NPL88		
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	NPL90		

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